SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF 2002-076334 3-15-02

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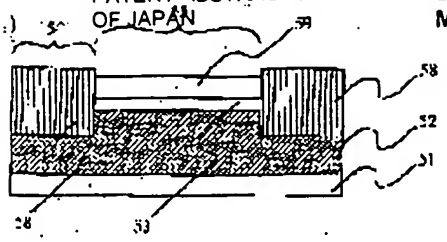

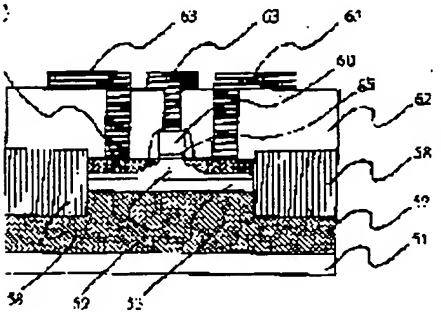

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(54) **SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREFOR**

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a semiconductor device having a high speed field effect transistor with low power consumption by using the combination of Si and Ge having the same family element as Si.
SOLUTION: The roughness of an interface between the distortion applying layer of SiGe and the distortion semiconductor layer of Si deposited thereon, or an interface between the distortion semiconductor layer of Si and the gate insulating layer on it are reduced to an appropriate value, and MOSFET is formed on the distortion semiconductor layer of Si.

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CLAIMS

[Claim(s)]
[Claim 1] The semiconductor device characterized by to consist of a gate electrode prepared in the front face of Si layer with a thickness of 100nm or less formed on the SiGe field formed in the substrate surface section, and the above-mentioned SiGe field, and the above-mentioned Si layer through the insulator layer, and to carry out flattening of the interface between the above-mentioned Si layer and the above-mentioned insulator layer with the relative-roughness power distribution property below 0.1 square NANOMETORU over the field under the above-mentioned gate electrode at least.
[Claim 2] The semiconductor device according to claim 1 characterized by carrying out flattening of the interface between the above-mentioned Si layer and the above-mentioned insulator layer with the relative roughness power distribution property below 0.02 square NANOMETORU over the field under the above-mentioned gate electrode at least.
[Claim 3] The manufacture method of the semiconductor device characterized by carrying out flattening of the front face of the SiGe field established in the substrate surface section by chemical machinery polish, depositing Si layer on the SiGe field by which flattening was carried out [above-mentioned], and forming an insulated-gate type transistor in the appropriate account Si layer of Gokami surface section.
[Claim 4] Thickness deposits the 1st Si layer 100 nanometers or less on the SiGe field established in the substrate front face. The circuit element isolation region which consists of an insulator partially is formed in the 1st Si layer and SiGe field by which deposition was carried out [above-mentioned]. The manufacture method of the semiconductor integrated circuit equipment characterized by for thickness depositing the 2nd Si layer 100 nanometers or less on the upper part of the appropriate 1st Si layer of the account of Gokami, and forming an insulated gate transistor in the above-mentioned 2nd Si layer.
[Claim 5] The high impurity concentration of the surface section of owner Perilla frutescens (L.) Britton var. crispa (Thunb.) Decne. the thickness of 100nm or less deposited on the SiGe field formed in the substrate surface section, and the above-mentioned SiGe field Si layer below the 17th power / cube cm of 10, And the semiconductor device which it consists of a gate electrode prepared in the surface upper part of the above-mentioned Si layer through the insulator layer, and the channel which has the carrier mobility 800 square centimeters / more than Vs is formed in the front face of the above-mentioned Si layer under the above-mentioned gate electrode, and is characterized by the bird clapper.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[The technical field to which invention belongs] this invention relates to a semiconductor device especially the semiconductor integrated circuit equipment containing an insulated gate transistor, and its manufacture method.
[0002]
[Description of the Prior Art] With the semiconductor integrated circuit equipment using the Si-MOS type field-effect transistor (Si-MOSFET), it has been compatible in reduction and improvement in the speed of power consumption by performing reduction of a device size, reduction of operating voltage, etc. according to the so-called scaling law. However, if it continues till recently and gate length is reduced to about 0.1 micrometers, many troubles, such as a problem of a short channel effect and a fall of the margin of operation by contiguity of drain voltage and threshold voltage, will arise.
[0003] Moreover, if their eyes are turned to the mobility used as the index of improvement in the speed, the above-mentioned various improvement has lapsed into the ironical result of reducing the mobility of Si in a real device further. Thus, in the conventional Si-MOSFET, the improvement in a performance is already becoming very difficult.
[0004] There is the need of attaining improvement in the speed by improvement of the semiconductor material itself in improvement in a performance beyond this. Although it is one solution, it is very difficult

to essentially use the so-called high-speed compound semiconductor in respect of fusion nature with the manufacturing technology of Si integrated circuit device, and since a manufacturing cost becomes huge, it is not a realistic solution.
[0005] Therefore, it is more realistic to offer the semiconductor device which has a high-speed field-effect transistor by the low power using the combination of germanium which is Si, and this and a congener.
[0006] Distortion is made to specifically impress to the channel cambium in which the channel of a field-effect transistor is formed by the distorted impression semiconductor layer, and it can attain by making mobility of the carrier in a channel larger than the material of a distortionlessness channel cambium. That is, when the material of a channel cambium is Si, the lattice constant within the field of Si channel cambium is made larger than distortionlessness Si by distorted impression.
[0007] if distortion is impressed to Si or germanium, the mobility of a carrier will increase compared with Si or germanium which does not receive distortion -- M.V.Fischetti andS.E.Laux:J.Appl.Phys. -- it is indicated by 80 (1996) and 2234
[0008]
[Problem(s) to be Solved by the Invention] As a method of giving distortion to Si layer, there is a method of growing up the SiGe mixed-crystal film of Si(1-x) germanium (x) of thickness sufficient on Si substrate, and growing up Si thin film on it further.
[0009] The lattice constant within a growth side of an Si(1-x) germanium(x) mixed-crystal film increases at the same time transition occurs in a film, in case the Si(1-x) germanium(x) mixed-crystal film of sufficient thickness is grown up, and it becomes of the same grade as bulk Si(1-x) germanium (x). That is, the grid mismatching of Si substrate and Si(1-x) germanium (x) film is eased. In this way, when Si film is grown up on the grown-up grid relief Si(1-x) germanium (x) film, the Si film will receive a tensile strain biaxial in a field.
[0010] However, that transition goes into an Si(1-x) germanium(x) mixed-crystal film for relief of grid mismatching lapses into the result which worsens remarkably the flat nature on the front face of a film simultaneously. Thus, even if it grows up a distorted Si layer to be the front face on which flat nature got worse and produces MOSFET, since dispersion of a carrier increases, the effect of mobility increase depended distorted will be offset, and it will have a bad influence also on detailed lithography indispensable to highly efficient element manufacture.
[0011] It is in offering the semiconductor device containing a distorted Si layer required for the 1st technical problem which this invention solves stopping performance aggravation of a device small, and performing a detailed lithography process.
[0012] The technical problem which should be solved when manufacturing the semiconductor device which contains a distorted Si layer in the 2nd is reducing the thermal load given to a distorted Si layer at the time of manufacture as much as possible. In the manufacturing process of the complementary-type field-effect transistor circuit apparatus which is the mainstream of a semiconductor device, a great thermal load is given in a well formation process and an isolation process. In the semiconductor substrate containing a distorted Si layer and a SiGe distorted impression layer, problems, such as diffusion of germanium from a SiGe distorted impression layer and strain relaxation of a distorted Si layer, may also produce the thermal load which is satisfactory in the single crystal Si substrate used conventionally. Therefore, reducing the influence of this thermal load is the 2nd technical problem which this invention solves.
[0013] Moreover, in order to acquire a good property by the short channel field-effect transistor, it is required to control the impurity profile of the channel field depth direction precisely. Although it is necessary to raise the high impurity concentration of the channel section for suppressing the punch-through current produced with short channelization, this reduces the effective mobility of a channel simultaneously and becomes the obstacle of the improvement in a property. Therefore, the high impurity concentration near [in which a channel is formed] a gate insulator layer interface is low, and control of the-like 3-dimensional impurity profile of making high high impurity concentration of a portion deeper than it becomes important.
[0014] Although control of an impurity profile was able to carry out comparatively easily by this method in the single crystal Si substrate conventionally used although how to pour into the depth which changes a 3 group element and a five-tribes element with ion-implantation can be considered, in the semiconductor substrate containing a distorted Si layer and a SiGe distorted impression layer, control

of an impurity profile becomes difficult by the anomalous diffusion of the dopant of a SiGe distorted impression layer. Avoiding this problem is the 3rd technical problem which this invention solves.
[0015] this invention is made for the purpose of solving the above 1 or the technical problem of 3, and offers the semiconductor integrated circuit equipment using the insulated gate transistor and it which improved the problem of a short channel effect and in which high-speed operation is possible.
[0016] Moreover, other purposes of this invention are also offering the manufacture method suitable for mass-producing this semiconductor device with sufficient repeatability.
[0017]
[Means for Solving the Problem] this invention is made paying attention to the influence the flat nature of the above-mentioned Si(1-x) germanium(x) mixed-crystal film surface affects an element property.
[0018] In order to solve the 1st technical problem of the above, this invention person etc. found out the need for carrying out flattening of the interface so that a relative roughness power distribution property (this is equivalent to the two-dimensional power spectral density of relative roughness.) may become below a predetermined size, as a result of repeating trial production examination per correlation of the relative roughness of the field side between the aforementioned layers, and a device property.
[0019] Especially, the influence of the relative roughness of the flat nature of the interface between the aforementioned distorted Si layer on SiGe and a gate insulator layer is size, and the need for carrying out flattening so that this interface, i.e., the relative roughness power distribution property of the flatness of Si layer, may become below a predetermined size was found out. Moreover, when the thickness of the aforementioned distorted Si layer was as thin as below 50 nanometers (nm), affecting similarly the relative roughness of the interface between the aforementioned SiGe distorted impression layer and a distorted Si layer remarkably was found out.
[0020] When the distribution to the wavelength (this is equivalent to the period of surface irregularity) of relative roughness power is seen, in a certain wavelength, it has a mountain (peak), and has the distribution which falls gently around it. Moreover, although it depends on the creation conditions of a sample, or the conditions of surface polish for the wavelength which shows the greatest relative roughness power At least specifically the flat nature of the interface between Si layer and a gate insulator layer A wavelength component the relative roughness power within the limits of 10 micrometers (micrometer) from 0.1 nanometers (nm) Below 0.1 square NANOMETORU (square nm) It found out that a good element property was acquired by making it desirable below 0.02 square NANOMETORU (square nm). Furthermore, when making flat nature of both the interface between Si layer and a gate insulator layer, and the interface between a SiGe distorted impression layer and Si layer into the above-mentioned range of number, that a further very good element property is acquired also found out again.
[0021] Moreover, performing flattening of the front face by the chemical machinery grinding method (CMP) in manufacture of the semiconductor device which has the laminated structure of the aforementioned Si substrate which fulfills such conditions, the distorted impression layer of an Si(1-x) germanium(x) mixed-crystal film (positive value with x [smaller than 1]), and Si distorted semiconductor layer, after growing up a ** and SiGe distorted impression layer on Si substrate found out the desirable thing.
[0022] In order to have solved the 2nd technical problem of the above, this invention person etc. found out that it is best to build a manufacturing process so that the process which gives a thermal load may be performed, before forming the aforementioned distorted Si layer. The concrete method is as follows.
[0023] First, the semiconductor substrate deposited on the aforementioned Si substrate in order of the Si(1-x) germanium(x) distorted impression layer and Si distorted semiconductor layer is manufactured. As for an Si(1-x) germanium(x) distorted impression layer and Si distorted semiconductor layer, it is desirable to make it grow up using methods, such as an ultra-high-vacuum exhaust air chemical-vapor-deposition method (UHVCVD). Moreover, although Si distorted semiconductor layer may not have this case, it is desirable to attach in order to use as the best front face Si layer which was excellent in chemical stability. Although the any value of 0 to 1 within the limits is possible for x which means the amount of germanium of a SiGe distorted impression layer, in respect of a deformation amount, 0.3 to about 0.4 are desirable. As for this x, it is also effective [decreasing the penetration dislocation density of a distorted impression layer], and desirable for there to be not necessarily no fixed need to the direction of thickness, and to enlarge x along with growth of a SiGe distorted impression layer.
[0024] Moreover, the aforementioned semiconductor substrate may be the so-called distorted

impression substrate of the SOI structure where insulating body whorls, such as SiO2, were inserted between for example, not only this combination but Si substrate, and the SiGe layer.
[0025] Next, a well formation process is given. Make the field which forms the N type transistor of the above-mentioned Si layer by methods, such as an ion implantation, dope a 3 group element, and make a conductivity type into P type, and the field which forms a P type transistor is made to dope a five-tribes element, and let a conductivity type be N type. One of processes may be skipped depending on the conductivity type and resistivity of Si layer to deposit.
[0026] Next, an isolation process is given to this semiconductor substrate. Methods, such as the local oxidizing [thermally] method (LOCOS) and trench separation, are applicable. When making the optimal the configuration of the difference of the height of the part for an insulating soma and the active region of an element which are formed at an isolation process, or a level difference and selection epitaxial growth of the Si layer is carried out at a next process, quality degradation of an epitaxial growth phase can be prevented by unusual formation, facet growth, etc. of the crystalline nucleus in an end face, and the property and isolation property of a transistor can be kept good.
[0027] Next, Si is grown epitaxially into the semiconductor substrate which passed through the well formation process and the isolation process. It is desirable to use the UHVCVD method with possible making it grow up to be only active regions other than an isolation field alternatively etc. for growth of this Si.
[0028] In addition, it is more desirable for etching to remove most 1st Si most [parts or] (in the case all), before forming the 2nd Si layer by epitaxial growth of Si, since germanium may be spread with the thermal load by the above-mentioned process in the 1st Si distorted semiconductor layer of the semiconductor substrate which passed through the above-mentioned well formation process. Moreover, growing up a SiGe layer in advance of growth of the 2nd Si layer can cover a surface contamination layer, and it is desirable.
[0029] By using the manufacture method which solves the 2nd technical problem of the above, the 3rd technical problem of the above also becomes solvable. That is, ion-implantation and heat treatment perform impurity addition so that the high impurity concentration of the 1st Si layer front face may become in the aforementioned well formation process the 17th power / more than the legislation cm of 10, after an appropriate time, in the epitaxial growth process of Above Si, low high impurity concentration is more required, and it is desirable to perform a process [need / precision to be controlled / an impurity profile] moreover, and to form the 2nd Si layer.
[0030] Or what is necessary is to perform impurity addition so that high impurity concentration may become in early stages of the epitaxial growth process of Si for forming the 2nd Si layer the 17th power / more than the legislation cm of 10, and just to perform impurity addition so that high impurity concentration may become below the 17th power / legislation cm of 10 after that. Since it is epitaxial growth of only Si and an impurity element, precise high-impurity-concentration control is attained compared with the case where both Si and germanium are included. In addition, the process which performs impurity addition so that high impurity concentration may become in early stages of the epitaxial growth process of Si the 17th power / more than the legislation cm of 10 may perform the process which performs impurity addition so that it may omit and high impurity concentration may become below the 17th power / legislation cm of 10 immediately depending on the case.
[0031] Anyway, it is desirable to make into below the 17th power / legislation cm of 10 high impurity concentration of Si layer surface section of the best layer in which an insulated gate transistor is formed.
[0032] In order not to ease distortion given by the aforementioned Si(1-x) germanium(x) distorted impression layer, it is desirable to make thickness of the aforementioned Si distorted semiconductor layer (1st Si layer) and an epitaxial Si layer (2nd Si layer) into the range of 1-100 nanometers (nm), respectively, and for the sum of the thickness of both layers to make it further the range of 1-100 nanometers (nm).
[0033] The SiGe field which has the flat front face formed in the substrate surface section according to this this invention, The high impurity concentration of the surface section of owner Perilla frutescens (L.) Britton var. crispa (Thunb.) Decne. the thickness of 100nm or less deposited on the above-mentioned SiGe field Si layer below the 17th power / cube cm of 10, And it consists of a gate electrode prepared in the surface upper part of the above-mentioned Si layer through the insulator layer, and the semiconductor device with which the channel which has the carrier mobility 800 square centimeters /

more than Vs was formed in the front face of the above-mentioned Si layer under the above-mentioned gate electrode can be realized.
[0034]
[Embodiments of the Invention] An example is given and explained about the relative roughness of the interface between a distorted Si layer required at the beginning of example 1 to solve the 1st technical problem of this invention, and a gate insulator layer, and the interface between a SiGe distorted impression layer and a distorted Si layer, and correlation of a device property.
[0035] First, the production method of an examination device is explained. An Si(1-x) germanium(x) distorted impression layer is first grown up on Si substrate by the ultra-high-vacuum exhaust air chemical-vapor-deposition method (UHVCVD). Flattening of the front face it was ruined with growth of this distorted impression layer is carried out with chemical machinery polish (CMP:Chemical Mechanical Polishing) technology.
[0036] Furthermore, in order to create various samples, some obtained samples split-face-ize a front face again by the chemical treatment etc., and control the surface roughness of a distorted impression layer to a desired value. Next, Si distorted semiconductor layer is grown up by the UHVCVD method on the SiGe distorted impression layer from which these surface roughness differs. Carrying out flattening of the front face by CMP again, some [further] samples are again split-face-ized by the chemical treatment, and also control the surface roughness of Si distorted semiconductor layer to a desired value.
[0037] In addition, the thickness of a SiGe distorted impression layer made 25 nanometers thickness of 3 micrometers and Si distorted semiconductor layer, and the germanium content x of a SiGe distorted impression layer made it increase continuously to 0 to 0.3, and the direction of thickness by the 2-micrometer first Atsushi, and was taken as the constant value of 0.3 by the remaining thickness of 1 micrometer.
[0038] Next, these samples were made to go via many processes of formation of gate SiO2 film by gate thermal oxidation, CVD of a polysilicon contest film, formation of the gate field by dry etching, the impurity ion implantation to a source drain field, layer insulation film formation, contact hole formation, and wiring formation one by one, and various MOSFETs for an examination were produced.
[0039] Evaluation of the relative roughness of the interface between a SiGe distorted impression layer and Si distorted semiconductor layer observed the sample surface roughness in front of Si distorted semiconductor stratification with the atomic force microscope (AFM), and was performed by the power spectrum calculation method according to ASTM E42.14 STM/AFM subcommittee advice. This It is called Power Spectral Density (PSD), FFT (fast Fourier transform) of the picture is squared for a picture, and it asks for the power P (unit; square nm).
[0040] Moreover, evaluation of the relative roughness of the interface between Si distorted semiconductor layer and a gate insulating layer removed the gate insulator layer by chemical etching, after performing gate thermal oxidation, and it was performed by similarly measuring surface roughness using AFM.
[0041] The property view (it is also called a power spectrum) which measured the power of relative roughness to the wavelength distribution which is equivalent to the irregularity of a SiGe distorted impression layer and the front face of Si distorted semiconductor layer interface at drawing 1 is shown. It controlled to four kinds of relative roughness so that it was shown by signs 11-14 all over drawing. The power spectrum of the relative roughness of Si distorted semiconductor layer and a gate insulating-layer interface is shown in drawing 2 . It controlled to four kinds of relative roughness as which it is similarly indicated here with signs 21-24. The combination of the relative roughness to 16 kinds of samples shown by this example is shown in Table 1.
[0042]
[Table 1]

[表1]

試料名	粗度1	粗度2
A	11	21
B	11	22
C	12	21
D	12	22
E	11	23
F	11	24
G	12	23
H	12	24
I	13	21
J	13	22
K	14	'21
L	14	22
M	13	23
N	13	24
O	14	23
P	14	24

[0043] In addition, all over the above-mentioned table, relative roughness 1 shows the relative roughness of a SiGe distorted impression layer and Si distorted semiconductor layer interface, relative roughness 2 shows the relative roughness of Si distorted semiconductor layer and a gate insulating-layer (SiO2 film) interface, and numbers 11-14, and 21-24 express the number of the characteristic curve attached in drawing 1 and drawing 2 , respectively.
[0044] ******** -- the electrical property of a sample with interface relative roughness is shown in drawing 3 The vertical axis of drawing 3 shows the effective mobility in the room temperature (27 degrees C) computed from the drain current characteristic of MOSFET, and the horizontal axis shows the field strength generated with gate-voltage impression. Effective mobility shows a high value, so that there is little dispersion of the carrier in an interface.
[0045] From this drawing 3 , like sample A-D, the mobility of a sample with the large relative roughness of both interfaces is the lowest, and the mobility of a sample with both small relative roughness becomes the highest like sample M-P. Although mobility falls [one of a distorted impression layer, a distorted semiconductor layer interface or a distorted semiconductor layer, and the insulator layer interfaces / rough ****** sample E-L], the property is improved for both rather than the rough ****** case.
[0046] That is, both of the interfaces are known by reducing the channel mobility of MOSFET by dispersion. Although drawing of this example showed only the case where the thickness of Si distorted semiconductor layer was 25 nanometers (nm), when the thickness of Si distorted semiconductor layer exceeded 50 nanometers (nm) from the result which examined many samples other than this, it became small [the influence which the relative roughness of a SiGe distorted impression layer and Si distorted semiconductor layer interface has on mobility] clearly rather [a bird clapper]. Moreover, in the interface of a SiGe distorted impression layer, Si distorted semiconductor layer interface and Si distorted semiconductor layer, or a gate insulator (SiO2 film) interface, relative roughness power came out of relative roughness required in order to make small influence which it has on mobility below 0.02 square NANOMETORU desirably below 0.1 square NANOMETORU over the wavelength range of 10 micrometers from 0.1nm, and a certain thing became clear.
[0047] Namely, by considering as flatness with the relative roughness power of above-mentioned [either the interface of a gate insulator layer and Si layer, and the interface of a SiGe layer and Si layer] within the limits, as shown in the sample E-L characteristic curve in drawing 3 , the field strength to a gate insulator layer is obtained with repeatability sufficient [the mobility of the channel section / MOSFET 400 square centimeters / more than Vs] in [of 6th power V/cm / practical use] 5 power -5x10 of 3x10.
[0048] Moreover, what the interface of a SiGe layer and Si layer is made into the flatness which had the

relative roughness power of above-mentioned within the limits beforehand for showed making into the relative roughness power of above-mentioned within the limits flatness of thin Si layer 100nm or less deposited on it, i.e., the flatness of the interface of a gate insulator layer and Si layer.
[0049] Moreover, by carrying out flatness of the interface of both above into the above-mentioned range of number, as shown in the sample M-P characteristic curve in drawing 3 , MOSFET which the mobility of the channel section excelled 800 square centimeters / more than Vs in the field strength to a gate insulator layer extremely in the practical use range of 6th power V/cm of 5 power -5x10 of 3x10 is obtained with sufficient repeatability.
[0050] The numerical range of the above-mentioned relative roughness power is shown in drawing 4 . It becomes so small that the fall of the mobility by dispersion can be disregarded if the relative roughness of a sample is in less than [the field which has performed hatching by drawing 4 , and it] (below). The reason the wavelength range of relative roughness is 10 micrometers or less and 0.1 nanometers or more is for hardly influencing a property, since it is larger than the size of a device, even if the former has the wave of a big period in a front face more than this, and since it becomes quite smaller than an electron wave function even if the irregularity of a short period is shown in a front face more than this, the latter is for not influencing dispersion of an electron wave.
The example of the manufacturing process of the semiconductor device which went to the well which solves the example 2 next the 2nd, and 3rd technical problems is shown below. The cross section of the semiconductor device in each process is shown in (4) of (1), (2), (3), and drawing 6 of drawing 5 , and (5).
[0051] First, the Si(1-x) germanium(x) distorted impression layer 52 is grown up by the UHVCVD method on the Si substrate 51. Flattening of the front face it was ruined with growth of the SiGe distorted impression layer 52 is carried out by CMP.
[0052] Next, the 1st Si layer (distorted semiconductor layer) 53 is grown up by the UHVCVD method on the SiGe distorted impression layer 52. In addition, the thickness of the distorted impression layer 52 of SiGe made 25 nanometers thickness of 3 micrometers and the distorted semiconductor layer 53 of Si, and the germanium content x of the distorted impression layer 52 made it increase continuously to the direction of thickness from zero to 0.3 by the first thickness of 2 micrometers, and was taken as the constant value of 0.3 by the remaining thickness of 1 micrometer. As the above process shows to (1) of drawing 5 , a distorted semiconductor substrate is prepared.
[0053] Next, a well formation process is given to this semiconductor substrate. It covers except the field which forms a P type transistor by photo lithography by the resist, and the ion implantation of Lynn is carried out, and let a conductivity type be N type. Similarly it covers except the field which forms an N type transistor by the resist, and the ion implantation of the boron is carried out, and let a conductivity type be P type. Moreover, in order to solve the 3rd technical problem of the above, surface high impurity concentration makes punch-through generating of a short channel element suppress at these processes, as 10 becomes higher than legislation cm the 17th whole power.
[0054] Next, the isolation field 54 is formed in this semiconductor substrate. In order to control the level difference of the isolation field 54 and an active region 55, after forming the thermal oxidation film (SiO2 film) 56 in the front face of Si distorted semiconductor layer 53, depositing the amorphous Si thin film 57 on it and covering except the front face of the isolation field 54 by the resist by photo lithography, it trenches [50 (trench)] by the reactive-ion-etching method. The state where the resist was furthermore removed is shown in (2) of drawing 5 .
[0055] Next, SiO2 film 58 is embedded in the above-mentioned trench by TEOS-CVD, and CMP performs flattening of these front faces. This state is shown in (3) of drawing 5 .
[0056] Furthermore, after etching or defecating the front face of the 1st Si layer (distorted semiconductor layer) 53 which removed the amorphous Si thin film 57 by reactive ion etching, removed the thermal oxidation film 56, and was exposed, Si is grown epitaxially by the UHVCVD method and the 2nd Si layer 59 is formed. In order to solve the 3rd technical problem of the above at this time, it controls to become below the 17th power / legislation cm of 10 about the high impurity concentration of a surface field portion, even if there are few these 2nd Si layers 59. This state is shown in (4) of drawing 6 .
[0057] next, each P type transistor field and N type transistor field -- the ion implantation for the object for threshold voltage adjustment and punch-through suppression is performed suitably independently
[0058] Henceforth, according to the usual CMOS transistor manufacture process, formation of the gate

thermal oxidation film (SiO2 film) 65, formation of the gate electrode 60 by CVD and dry etching of a polysilicon contest film, formation of the source drain field 61 by the impurity ion implantation, formation of the layer insulation film 62, formation of a contact hole, and formation of the source drain gate electrode wiring 63 are performed, and the semiconductor device concerning this invention is completed. The cross section of the completion state is shown in (5) of drawing 6 .
[0059] The transistor completed through the above process Distortion is impressed to the channel formation field 53 of Si on it by the distorted impression layer 52 of SiGe, It is appropriately controlled by suitable CMP, the relative roughness, i.e., the flatness, of those interfaces Namely, it sets to one [at least] interface of the interface of the interface of a SiGe distorted impression layer and Si distorted semiconductor layer, Si distorted semiconductor layer, and a gate insulator (SiO2 film). Relative roughness power made it desirable below 0.02 square NANOMETORU below 0.1 square NANOMETORU over the wavelength range of 10 micrometers from 0.1nm, It is the Si epitaxial growth phase 59 (since a gate electrode is formed in the upper part of the front face, this layer) after well formation or an isolation process. as the active region or channel formation field of a transistor -- functioning -- by having controlled and formed high impurity concentration and having suppressed the fall of the mobility by the short channel effect and the impurity Compared with the element by the usual Si substrate which gave the same process, the current drive capacity more than double precision and a high working speed are realizable.
[0060] By manufacturing a semiconductor integrated circuit with the application of such this invention, since improvement in the speed, high integration, and highly efficient-ization can be attained, the industrial value is very high.
[0061] If it carries out as a substrate using Si wafer as the above example explained, by combining suitably the usual IC, the manufacturing process of LSI, and the manufacturing process of this invention, it can unite with usual IC and usual LSI, and can depend, and highly efficient LSI can be realized.
[0062] Moreover, since the carrier mobility of the channel section can make the thing more than 400 square cm/Vs, and the thing more than 800 more square cm/Vs with sufficient repeatability according to this invention even if it is MOSFET of a P type channel and is MOSFET of an N type channel so that I may be understood from having described above, the semiconductor integrated circuit equipment of the CMOS type with which especially the high-speed operation in a low power is demanded is realizable.
[0063] Moreover, CMOSLSI to which it becomes easy to carry out also arranging the mobility of PCHANERU type and both N channel type MOSFETs with the above-mentioned predetermined value in that case and the circuit design of CMOSLSI which achieves a highly efficient and complicated function since it becomes possible, and the carrier mobility property was equal becomes possible.
[0064]
[Effect of the Invention] According to this invention, dispersion accompanying the formation of an interface split face by introducing the distorted semiconductor of Si can be suppressed, and the semiconductor integrated circuit equipment which was excellent in the property constituted from high speed, a complementary-type field-effect transistor of a low power, and it can be realized.

[Translation done.]

TECHNICAL FIELD

[The technical field to which invention belongs] this invention relates to a semiconductor device especially the semiconductor integrated circuit equipment containing an insulated gate transistor, and its manufacture method.

[Translation done.]

PRIOR ART

[Description of the Prior Art] With the semiconductor integrated circuit equipment using the Si-MOS type field-effect transistor (Si-MOSFET), it has been compatible in reduction and improvement in the speed of power consumption by performing reduction of a device size, reduction of operating voltage, etc. according to the so-called scaling law. However, if it continues till recently and gate length is reduced to about 0.1 micrometers, many troubles, such as a problem of a short channel effect and a fall of the margin of operation by proximity of drain voltage and threshold voltage, will arise.
[0003] Moreover, if their eyes are turned to the mobility used as the index of improvement in the speed, the above-mentioned various improvement has lapsed into the ironical result of reducing the mobility of Si in a real device further. Thus, in the conventional Si-MOSFET, the improvement in a performance is already becoming very difficult.
[0004] There is the need of attaining improvement in the speed by improvement of the semiconductor material itself in improvement in a performance beyond this. Although it is one solution, it is very difficult to essentially use the so-called high-speed compound semiconductor in respect of fusion nature with the manufacturing technology of Si integrated circuit device, and since a manufacturing cost becomes huge, it is not a realistic solution.
[0005] Therefore, it is more realistic to offer the semiconductor device which has a high-speed field-effect transistor by the low power using the combination of germanium which is Si, and this and a congener.
[0006] Distortion is made to specifically impress to the channel cambium in which the channel of a field-effect transistor is formed by the distorted impression semiconductor layer, and it can attain by making mobility of the carrier in a channel larger than the material of a distortionlessness channel cambium. That is, when the material of a channel cambium is Si, the lattice constant within the field of Si channel cambium is made larger than distortionlessness Si by distorted impression.
[0007] if distortion is impressed to Si or germanium, the mobility of a carrier will increase compared with Si or germanium which does not receive distortion -- M.V.Fischetti andS.E.Laux:J.Appl.Phys. -- it is indicated by 80 (1996) and 2234

[Translation done.]

EFFECT OF THE INVENTION

[Effect of the Invention] According to this invention, dispersion accompanying the formation of an interface split face by introducing the distorted semiconductor of Si can be suppressed, and the semiconductor integrated circuit equipment which was excellent in the property constituted from high speed, a complementary-type field-effect transistor of a low power, and it can be realized.

[Translation done.]

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] As a method of giving distortion to Si layer, there is a method of growing up the SiGe mixed-crystal film of Si(1-x) germanium (x) of thickness sufficient on Si substrate, and growing up Si thin film on it further.
[0009] The lattice constant within a growth side of an Si(1-x) germanium(x) mixed-crystal film increases at the same time transition occurs in a film, in case the Si(1-x) germanium(x) mixed-crystal film of sufficient thickness is grown up, and it becomes of the same grade as bulk Si(1-x) germanium (x). That is, the grid mismatching of Si substrate and Si(1-x) germanium (x) film is eased. In this way, when Si film is grown up on the grown-up grid relief Si(1-x) germanium (x) film, the Si film will receive a tensile strain biaxial in a field.
[0010] However, that transition goes into an Si(1-x) germanium(x) mixed-crystal film for relief of grid

mismatching lapses into the result which worsens remarkably the flat nature on the front face of a film simultaneously. Thus, even if it grows up a distorted Si layer to be the front face on which flat nature got worse and produces MOSFET, since dispersion of a carrier increases, the effect of mobility increase depended distorted will be offset, and it will have a bad influence also on detailed lithography indispensable to highly efficient element manufacture.
[0011] It is in offering the semiconductor device containing a distorted Si layer required for the 1st technical problem which this invention solves stopping performance aggravation of a device small, and performing a detailed lithography process.
[0012] The technical problem which should be solved when manufacturing the semiconductor device which contains a distorted Si layer in the 2nd is reducing the thermal load given to a distorted Si layer at the time of manufacture as much as possible. In the manufacturing process of the complementary-type field-effect transistor circuit apparatus which is the mainstream of a semiconductor device, a great thermal load is given in a well formation process and an isolation process. In the semiconductor substrate containing a distorted Si layer and a SiGe distorted impression layer, problems, such as diffusion of germanium from a SiGe distorted impression layer and strain relaxation of a distorted Si layer, may also produce the thermal load which is satisfactory in the single crystal Si substrate used conventionally. Therefore, reducing the influence of this thermal load is the 2nd technical problem which this invention solves.
[0013] Moreover, in order to acquire a good property by the short channel field-effect transistor, it is required to control the impurity profile of the channel field depth direction precisely. Although it is necessary to raise the high impurity concentration of the channel section for suppressing the punch-through current produced with short channelization, this reduces the effective mobility of a channel simultaneously and becomes the obstacle of the improvement in a property. Therefore, the high impurity concentration near [in which a channel is formed] a gate insulator layer interface is low, and control of the-like 3-dimensional impurity profile of making high high impurity concentration of a portion deeper than it becomes important.
[0014] Although control of an impurity profile was able to carry out comparatively easily by this method in the single crystal Si substrate conventionally used although how to pour into the depth which changes a 3 group element and a five-tribes element with ion-implantation can be considered, in the semiconductor substrate containing a distorted Si layer and a SiGe distorted impression layer, control of an impurity profile becomes difficult by the anomalous diffusion of the dopant of a SiGe distorted impression layer. Avoiding this problem is the 3rd technical problem which this invention solves.
[0015] this invention is made for the purpose of solving the above 1 or the technical problem of 3, and offers the semiconductor integrated circuit equipment using the insulated gate transistor and it which improved the problem of a short channel effect and in which high-speed operation is possible.
[0016] Moreover, other purposes of this invention are also offering the manufacture method suitable for mass-producing this semiconductor device with sufficient repeatability.

[Translation done.]

MEANS

[Means for Solving the Problem] this invention is made paying attention to the influence the flat nature of the above-mentioned Si(1-x) germanium(x) mixed-crystal film surface affects an element property.
[0018] In order to solve the 1st technical problem of the above, this invention person etc. found out the need for carrying out flattening of the interface so that a relative roughness power distribution property (this is equivalent to the two-dimensional power spectral density of relative roughness.) may become below a predetermined size, as a result of repeating trial production examination per correlation of the relative roughness of the field side between the aforementioned layers, and a device property.
[0019] Especially, the influence of the relative roughness of the flat nature of the interface between the aforementioned distorted Si layer on SiGe and a gate insulator layer is size, and the need for carrying out flattening so that this interface, i.e., the relative roughness power distribution property of the flatness of Si layer, may become below a predetermined size was found out. Moreover, when the thickness of

the aforementioned distorted Si layer was as thin as below 50 nanometers (nm), affecting similarly the relative roughness of the interface between the aforementioned SiGe distorted impression layer and a distorted Si layer remarkably was found out.
[0020] When the distribution to the wavelength (this is equivalent to the period of surface irregularity) of relative roughness power is seen, in a certain wavelength, it has a mountain (peak), and has the distribution which falls gently around it. Moreover, although it depends on the creation conditions of a sample, or the conditions of surface polish for the wavelength which shows the greatest relative roughness power At least specifically the flat nature of the interface between Si layer and a gate insulator layer A wavelength component the relative roughness power within the limits of 10 micrometers (micrometer) from 0.1 nanometers (nm) Below 0.1 square NANOMETORU (square nm) It found out that a good element property was acquired by making it desirable below 0.02 square NANOMETORU (square nm). Furthermore, when making flat nature of both the interface between Si layer and a gate insulator layer, and the interface between a SiGe distorted impression layer and Si layer into the above-mentioned range of number, that a further very good element property is acquired also found out again.
[0021] Moreover, performing flattening of the front face by the chemical machinery grinding method (CMP) in manufacture of the semiconductor device which has the laminated structure of the aforementioned Si substrate which fulfills such conditions, the distorted impression layer of an Si(1-x) germanium(x) mixed-crystal film (positive value with x [smaller than 1]), and Si distorted semiconductor layer, after growing up a ** and SiGe distorted impression layer on Si substrate found out the desirable thing.
[0022] In order to have solved the 2nd technical problem of the above, this invention person etc. found out that it is best to build a manufacturing process so that the process which gives a thermal load may be performed, before forming the aforementioned distorted Si layer. The concrete method is as follows.
[0023] First, the semiconductor substrate deposited on the aforementioned Si substrate in order of the Si(1-x) germanium(x) distorted impression layer and Si distorted semiconductor layer is manufactured. As for an Si(1-x) germanium(x) distorted impression layer and Si distorted semiconductor layer, it is desirable to make it grow up using methods, such as an ultra-high-vacuum exhaust air chemical-vapor-deposition method (UHVCVD). Moreover, although Si distorted semiconductor layer may not have this case, it is desirable to attach in order to use as the best front face Si layer which was excellent in chemical stability. Although the any value of 0 to 1 within the limits is possible for x which means the amount of germanium of a SiGe distorted impression layer, in respect of a deformation amount, 0.3 to about 0.4 are desirable. As for this x, it is also effective [decreasing the penetration dislocation density of a distorted impression layer], and desirable for there to be not necessarily no fixed need to the direction of thickness, and to enlarge x along with growth of a SiGe distorted impression layer.
[0024] Moreover, the aforementioned semiconductor substrate may be the so-called distorted impression substrate of the SOI structure where insulating body whorls, such as SiO2, were inserted between for example, not only this combination but Si substrate, and the SiGe layer.
[0025] Next, a well formation process is given. Make the field which forms the N type transistor of the above-mentioned Si layer by methods, such as an ion implantation, dope a 3 group element, and make a conductivity type into P type, and the field which forms a P type transistor is made to dope a five-tribes element, and let a conductivity type be N type. One of processes may be skipped depending on the conductivity type and resistivity of Si layer to deposit.
[0026] Next, an isolation process is given to this semiconductor substrate. Methods, such as the local oxidizing [thermally] method (LOCOS) and trench separation, are applicable. When making the optimal the configuration of the difference of the height of the part for an insulating soma and the active region of an element which are formed at an isolation process, or a level difference and selection epitaxial growth of the Si layer is carried out at a next process, quality degradation of an epitaxial growth phase can be prevented by unusual formation, facet growth, etc. of the crystalline nucleus in an end face, and the property and isolation property of a transistor can be kept good.
[0027] Next, Si is grown epitaxially into the semiconductor substrate which passed through the well formation process and the isolation process. It is desirable to use the UHVCVD method with possible making it grow up to be only active regions other than an isolation field alternatively etc. for growth of this Si.
[0028] In addition, it is more desirable for etching to remove most 1st Si most [parts or] (in the case

all), before forming the 2nd Si layer by epitaxial growth of Si, since germanium may be spread with the thermal load by the above-mentioned process in the 1st Si distorted semiconductor layer of the semiconductor substrate which passed through the above-mentioned well formation process. Moreover, growing up a SiGe layer in advance of growth of the 2nd Si layer can cover a surface contamination layer, and it is desirable.

[0029] By using the manufacture method which solves the 2nd technical problem of the above, the 3rd technical problem of the above also becomes solvable. That is, ion-implantation and heat treatment perform impurity addition so that the high impurity concentration of the 1st Si layer front face may become in the aforementioned well formation process the 17th power / more than the legislation cm of 10, after an appropriate time, in the epitaxial growth process of Above Si, lower high impurity concentration is required and it is desirable to perform a process [need / precision to be controlled / an impurity profile] moreover, and to form the 2nd Si layer.

[0030] Or what is necessary is to perform impurity addition so that high impurity concentration may become in early stages of the epitaxial growth process of Si for forming the 2nd Si layer the 17th power / more than the legislation cm of 10, and just to perform impurity addition so that high impurity concentration may become below the 17th power / legislation cm of 10 after that. Since it is epitaxial growth of only Si and an impurity element, precise high-impurity-concentration control is attained compared with the case where both Si and germanium are included. In addition, the process which performs impurity addition so that high impurity concentration may become in early stages of the epitaxial growth process of Si the 17th power / more than the legislation cm of 10 may perform the process which performs impurity addition so that it may omit and high impurity concentration may become below the 17th power / legislation cm of 10 immediately depending on the case.

[0031] Anyway, it is desirable to make into below the 17th power / legislation cm of 10 high impurity concentration of Si layer surface section of the best layer in which an insulated gate transistor is formed.

[0032] In order not to ease distortion given by the aforementioned Si(1-x) germanium(x) distorted impression layer, it is desirable to make thickness of the aforementioned Si distorted semiconductor layer (1st Si layer) and an epitaxial Si layer (2nd Si layer) into the range of 1-100nm (nm), respectively, and for the sum of the thickness of both layers to make it further the range of 1-100nm (nm).

[0033] The SiGe field which has the flat front face formed in the substrate surface section according to this this invention, The high impurity concentration of the surface section of owner Perilla frutescens (L.) Britton var. crispa (Thunb.) Decne. the thickness of 100nm or less deposited on the above-mentioned SiGe field Si layer below the 17th power / cube cm of 10, And it consists of a gate electrode prepared in the surface upper part of the above-mentioned Si layer through the insulator layer, and the semiconductor device with which the channel which has the carrier mobility 800 square centimeters / more than Vs was formed in the front face of the above-mentioned Si layer under the above-mentioned gate electrode can be realized.

[0034]

[Embodiments of the Invention] An example is given and explained about the relative roughness of the interface between a distorted Si layer required at the beginning of example 1 to solve the 1st technical problem of this invention, and a gate insulator layer, and the interface between a SiGe distorted impression layer and a distorted Si layer, and correlation of a device property.

[0035] First, the production method of an examination device is explained. An Si(1-x) germanium(x) distorted impression layer is first grown up on Si substrate by the ultra-high-vacuum exhaust air chemical-vapor-deposition method (UHVCVD). Flattening of the front face it was ruined with growth of this distorted impression layer is carried out with chemical machinery polish (CMP:Chemical Mechanical Polishing) technology.

[0036] Furthermore, in order to create various samples, some obtained samples split-face-ize a front face again by the chemical treatment etc., and control the surface roughness of a distorted impression layer to a desired value. Next, Si distorted semiconductor layer is grown up by the UHVCVD method on the SiGe distorted impression layer from which these surface roughness differs. Carrying out flattening of the front face by CMP again, some [further] samples are again split-face-ized by the chemical treatment, and also control the surface roughness of Si distorted semiconductor layer to a desired value.

[0037] In addition, the thickness of a SiGe distorted impression layer made 25nm thickness of 3

micrometers and Si distorted semiconductor layer, and the germanium content x of a SiGe distorted impression layer made it increase continuously to 0 to 0.3, and the direction of thickness by the 2-micrometer first Atsushi, and was taken as the constant value of 0.3 by the remaining thickness of 1 micrometer.

[0038] Next, these samples were made to go via many processes of formation of gate SiO2 film by gate thermal oxidation, CVD of a polysilicon contest film, formation of the gate field by dry etching, the impurity ion implantation to a source drain field, layer insulation film formation, contact hole formation, and wiring formation one by one, and various MOSFETs for an examination were produced.

[0039] Evaluation of the relative roughness of the interface between a SiGe distorted impression layer and Si distorted semiconductor layer observed the sample surface roughness in front of Si distorted semiconductor layer formation with the atomic force microscope (AFM), and was performed by the power spectrum calculation method according to ASTM E42.14 STM/AFM subcommittee advice. This It is called Power Spectral Density (PSD), FFT (fast Fourier transform) of the picture is squared for a picture, and it asks for the power P (unit; square nm).

[0040] Moreover, evaluation of the relative roughness of the interface between Si distorted semiconductor layer and a gate insulating layer removed the gate insulator layer by chemical etching, after performing gate thermal oxidation, and it was performed by similarly measuring surface roughness using AFM.

[0041] The property view (it is also called a power spectrum) which measured the power of relative roughness to the wavelength distribution which is equivalent to the irregularity of a SiGe distorted impression layer and the front face of Si distorted semiconductor layer interface at drawing 1 is shown. It controlled to four kinds of relative roughness so that it was shown by signs 11-14 all over drawing. The power spectrum of the relative roughness of Si distorted semiconductor layer and a gate insulating-layer interface is shown in drawing 2 . It controlled to four kinds of relative roughness as which it is similarly indicated here with signs 21-24. The combination of the relative roughness to 16 kinds of samples shown by this example is shown in Table 1.

[0042]

[Table 1]

[表1]

試料名	粗度1	粗度2
A	11	21
B	11	22
C	12	21
D	12	22
E	11	23
F	11	24
G	12	23
H	12	24
I	13	21
J	13	22
K	14	21
L	14	22
M	13	23
N	13	24
O	14	23
P	14	24

[0043] In addition, all over the above-mentioned table, relative roughness 1 shows the relative roughness of a SiGe distorted impression layer and Si distorted semiconductor layer interface, relative roughness 2 shows the relative roughness of Si distorted semiconductor layer and a gate insulating-layer (SiO2 film) interface, and numbers 11-14, and 21-24 express the number of the characteristic curve attached in drawing 1 and drawing 2 , respectively.

[0044] ******** -- the electrical property of a sample with interface relative roughness is shown in

drawing 3 The vertical axis of drawing 3 shows the effective mobility in the room temperature (27 degrees C) computed from the drain current characteristic of MOSFET, and the horizontal axis shows the field strength generated with gate-voltage impression. Effective mobility shows a high value, so that there is little dispersion of the carrier in an interface.

[0045] From this drawing 3 , like sample A-D, the mobility of a sample with the large relative roughness of both interfaces is the lowest, and the mobility of a sample with both small relative roughness becomes the highest like sample M-P. Although mobility falls [one of a distorted impression layer, a distorted semiconductor layer interface or a distorted semiconductor layer, and the insulator layer interfaces / rough ****** sample E-L], the property is improved for both rather than the rough ****** case.

[0046] That is, both of the interfaces are known by reducing the channel mobility of MOSFET by dispersion. Although drawing of this example showed only the case where the thickness of Si distorted semiconductor layer was 25 nanometers (nm), when the thickness of Si distorted semiconductor layer exceeded 50 nanometers (nm) from the result which examined many samples other than this, it became small [the influence which the relative roughness of a SiGe distorted impression layer and Si distorted semiconductor layer interface has on mobility] clearly rather [a bird clapper]. Moreover, in the interface of a SiGe distorted impression layer, Si distorted semiconductor layer interface and Si distorted semiconductor layer, or a gate insulator (SiO2 film) interface, relative roughness power came out of relative roughness required in order to make small influence which it has on mobility below 0.02 square NANOMETORU desirably below 0.1 square NANOMETORU over the wavelength range of 10 micrometers from 0.1nm, and a certain thing became clear.

[0047] Namely, by considering as flatness with the relative roughness power of above-mentioned [either the interface of a gate insulator layer and Si layer, and the interface of a SiGe layer and Si layer] within the limits, as shown in the sample E-L characteristic curve in drawing 3 , the field strength to a gate insulator layer is obtained with repeatability sufficient [the mobility of the channel section / MOSFET 400 square centimeters / more than Vs] in [of 6th power V/cm / practical use] 5 power -5x10 of 3x10.

[0048] Moreover, what the interface of a SiGe layer and Si layer is made into the flatness which had the relative roughness power of above-mentioned within the limits beforehand for showed making into the relative roughness power of above-mentioned within the limits flatness of thin Si layer 100nm or less deposited on it, i.e., the flatness of the interface of a gate insulator layer and Si layer.

[0049] Moreover, by carrying out flatness of the interface of both above into the above-mentioned range of number, as shown in the sample M-P characteristic curve in drawing 3 , MOSFET which the mobility of the channel section excelled 800 square centimeters / more than Vs in the field strength to a gate insulator layer extremely in the practical use range of 6th power V/cm of 5 power -5x10 of 3x10 is obtained with sufficient repeatability.

[0050] The numerical range of the above-mentioned relative roughness power is shown in drawing 4 . It becomes so small that the fall of the mobility by dispersion can be disregarded if the relative roughness of a sample is in less than [the field which has performed hatching by drawing 4 , and it] (below). The reason the wavelength range of relative roughness is 10 micrometers or less and 0.1nm or more is for hardly influencing a property, since it is larger than the size of a device, even if the former has the wave of a big period in a front face more than this, and since it becomes quite smaller than an electron wave function even if the irregularity of a short period is shown in a front face more than this, the latter is for not influencing dispersion of an electron wave.

The example of the manufacturing process of the semiconductor device which went to the well which solves the example 2 next the 2nd, and 3rd technical problems is shown below. The cross section of the semiconductor device in each process is shown in (4) of (1), (2), (3), and drawing 6 of drawing 5 , and (5).

[0051] First, the Si(1-x) germanium(x) distorted impression layer 52 is grown up by the UHVCVD method on the Si substrate 51. Flattening of the front face it was ruined with growth of the SiGe distorted impression layer 52 is carried out by CMP.

[0052] Next, the 1st Si layer (distorted semiconductor layer) 53 is grown up by the UHVCVD method on the SiGe distorted impression layer 52. In addition, the thickness of the distorted impression layer 52 of SiGe made 25nm thickness of 3 micrometers and the distorted semiconductor layer 53 of Si, and the germanium content x of the distorted impression layer 52 made it increase continuously to the direction

of thickness from zero to 0.3 by the first thickness of 2 micrometers, and was taken as the constant value of 0.3 by the remaining thickness of 1 micrometer. As the above process shows to (1) of drawing 5 , a distorted semiconductor substrate is prepared.
[0053] Next, a well formation process is given to this semiconductor substrate. It covers except the field which forms a P type transistor by photo lithography by the resist, and the ion implantation of Lynn is carried out, and let a conductivity type be N type. Similarly it covers except the field which forms an N type transistor by the resist, and the ion implantation of the boron is carried out, and let a conductivity type be P type. Moreover, in order to solve the 3rd technical problem of the above, surface high impurity concentration makes punch-through generating of a short channel element suppress at these processes, as 10 becomes higher than legislation cm the 17th whole power.
[0054] Next, the isolation field 54 is formed in this semiconductor substrate. In order to control the level difference of the isolation field 54 and an active region 55, after forming the thermal oxidation film (SiO2 film) 56 in the front face of Si distorted semiconductor layer 53, depositing the amorphous Si thin film 57 on it and covering except the front face of the isolation field 54 by the resist by photo lithography, it trenches [50 (trench)] by the reactive-ion-etching method. The state where the resist was furthermore removed is shown in (2) of drawing 5 .
[0055] Next, SiO2 film 58 is embedded in the above-mentioned trench by TEOS-CVD, and CMP performs flattening of these front faces. This state is shown in (3) of drawing 5 .
[0056] Furthermore, after etching or defecating the front face of the 1st Si layer (distorted semiconductor layer) 53 which removed the amorphous Si thin film 57 by reactive ion etching, removed the thermal oxidation film 56, and was exposed, Si is grown epitaxially by the UHVCVD method and the 2nd Si layer 59 is formed. In order to solve the 3rd technical problem of the above at this time, it controls to become below the 17th power / legislation cm of 10 about the high impurity concentration of a surface field portion, even if there are few these 2nd Si layers 59. This state is shown in (4) of drawing 6 .
[0057] next, each P type transistor field and N type transistor field -- the ion implantation for the object for threshold voltage adjustment and punch-through suppression is performed suitably independently
[0058] Henceforth, according to the usual CMOS transistor manufacture process, formation of the gate thermal oxidation film (SiO2 film) 65, formation of the gate electrode 60 by CVD and dry etching of a polysilicon contest film, formation of the source drain field 61 by the impurity ion implantation. formation of the layer insulation film 62, formation of a contact hole, and formation of the source drain gate electrode wiring 63 are performed, and the semiconductor device concerning this invention is completed. The cross section of the completion state is shown in (5) of drawing 6 .
[0059] The transistor completed through the above process Distortion is impressed to the channel formation field 53 of Si on it by the distorted impression layer 52 of SiGe, It is appropriately controlled by suitable CMP, the relative roughness, i.e., the flatness, of those interfaces Namely, it sets to one [at least] interface of the interface of the interface of a SiGe distorted impression layer and Si distorted semiconductor layer, Si distorted semiconductor layer, and a gate insulator (SiO2 film). Relative roughness power made it desirable below 0.02 square NANOMETORU below 0.1 square NANOMETORU over the wavelength range of 10 micrometers from 0.1nm, It is the Si epitaxial growth phase 59 (since a gate electrode is formed in the upper part of the front face, this layer) after well formation or an isolation process. as the active region or channel formation field of a transistor -- functioning -- by having controlled and formed high impurity concentration and having suppressed the fall of the mobility by the short channel effect and the impurity Compared with the element by the usual Si substrate which gave the same process, the current drive capacity more than double precision and a high working speed are realizable.
[0060] By manufacturing a semiconductor integrated circuit with the application of such this invention, since improvement in the speed, high integration, and highly efficient-ization can be attained, the industrial value is very high.
[0061] If it carries out as a substrate using Si wafer as the above example explained, by combining suitably the usual IC, the manufacturing process of LSI, and the manufacturing process of this invention, it can unite with usual IC and usual LSI, and can depend, and highly efficient LSI can be realized.
[0062] Moreover, since the carrier mobility of the channel section can make the thing more than 400 square cm/Vs, and the thing more than 800 more square cm/Vs with sufficient repeatability according to

this invention even if it is MOSFET of a P type channel and is MOSFET of an N type channel so that I may be understood from having described above, the semiconductor integrated circuit equipment of the CMOS type with which especially the high-speed operation in a low power is demanded is realizable.
[0063] Moreover, CMOSLSI to which it becomes easy to carry out also arranging the mobility of PCHANERU type and both N channel type MOSFETs with the above-mentioned predetermined value in that case and the circuit design of CMOSLSI which achieves a highly efficient and complicated function since it becomes possible, and the carrier mobility property was equal becomes possible.

[Translation done.]

DESCRIPTION OF DRAWINGS

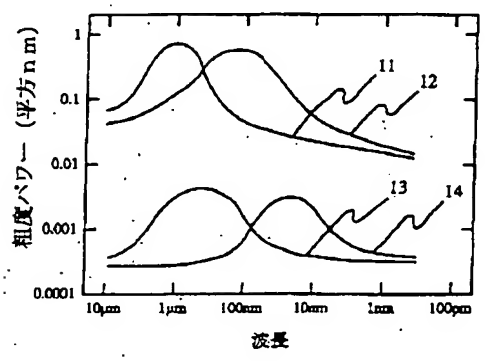
[Brief Description of the Drawings]
[Drawing 1] It is the power spectrum property view of the relative roughness of the interface between the SiGe distorted impression layers and Si distorted semiconductor layers concerning this invention.
[Drawing 2] It is the power spectrum property view of the relative roughness of the interface between Si distorted semiconductor layers and the gate insulating layers concerning this invention.
[Drawing 3] It is the property view showing the mobility property of various samples of having different interface relative roughness in the example 1 of this invention.
[Drawing 4] It is a property view for explaining the field of the relative roughness of a SiGe distorted impression layer and Si distorted semiconductor layer interface required to acquire the good mobility property in the example 1 of this invention, and an Si distorted semiconductor layer and a gate insulating-layer interface.
[Drawing 5] It is the cross section showing the manufacturing process of the field-effect transistor shown in the example 2 of this invention.
[Drawing 6] It is the cross section showing the manufacturing process of the field-effect transistor shown in the example 2 of this invention.
[Description of Notations]
50 [-- A SiGe distorted impression layer, 53 / -- The 1st Si layer (distorted semiconductor layer), 54 / -- An isolation field, 55 / -- An active region, 56 / -- A thermal oxidation film, 57 / -- An amorphous Si thin film, 58 / -- A SiO2 trench embedding film, 59 / -- The 2nd Si layer (Si epitaxial growth phase), 61 / -- A source drain semiconductor region, 60 / -- A gate electrode, 65] -- A trench, 51 -- Si substrate, 52

[Translation done.]

DRAWINGS

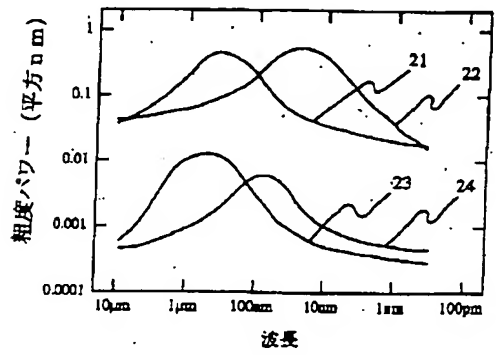
[Drawing 1]

図1



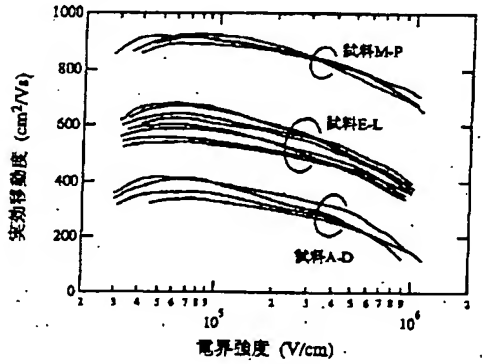
[Drawing 2]

図2



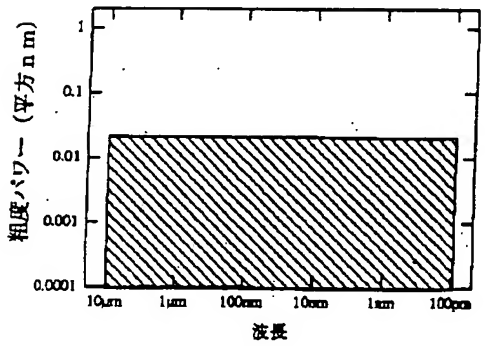
[Drawing 3]

図3



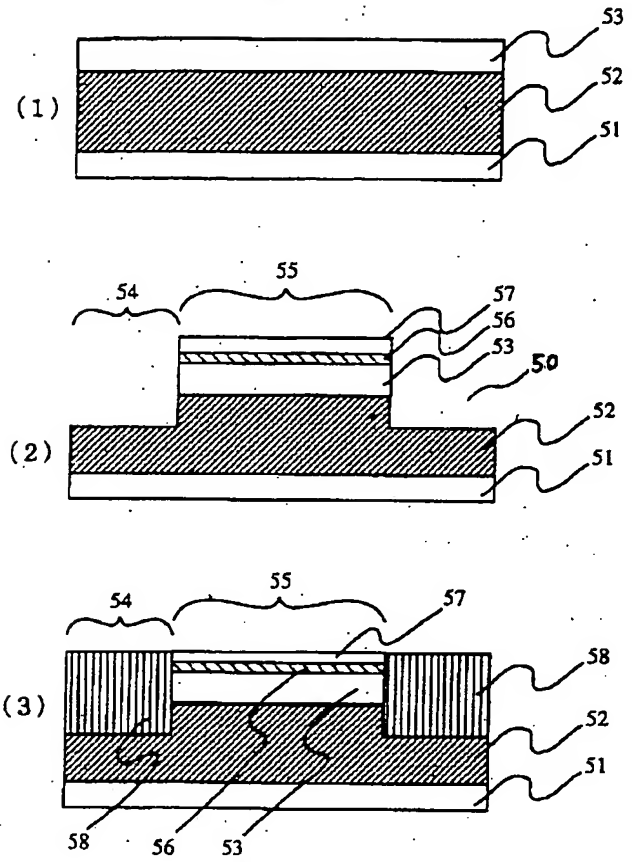
[Drawing 4]

図4



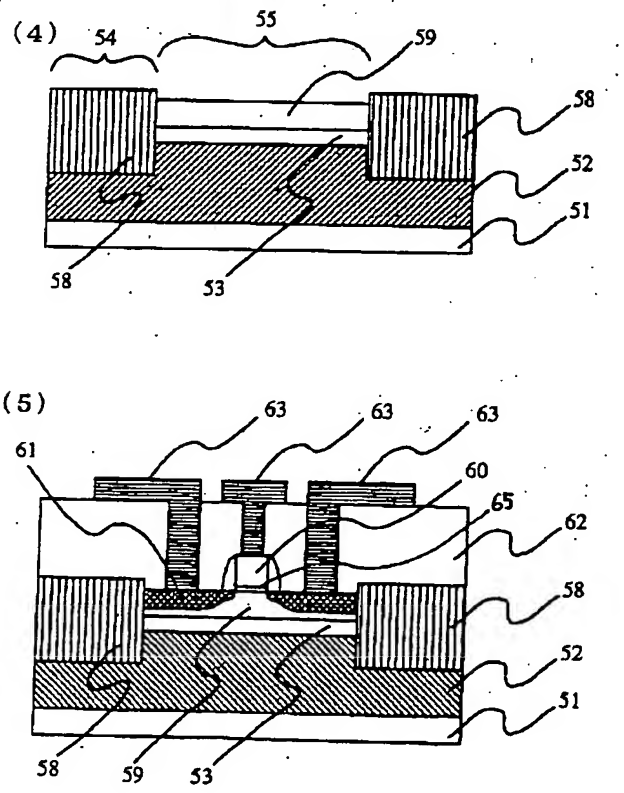
[Drawing 5]

図5



[Drawing 6]

図6



[Translation done.]